FIG. 1

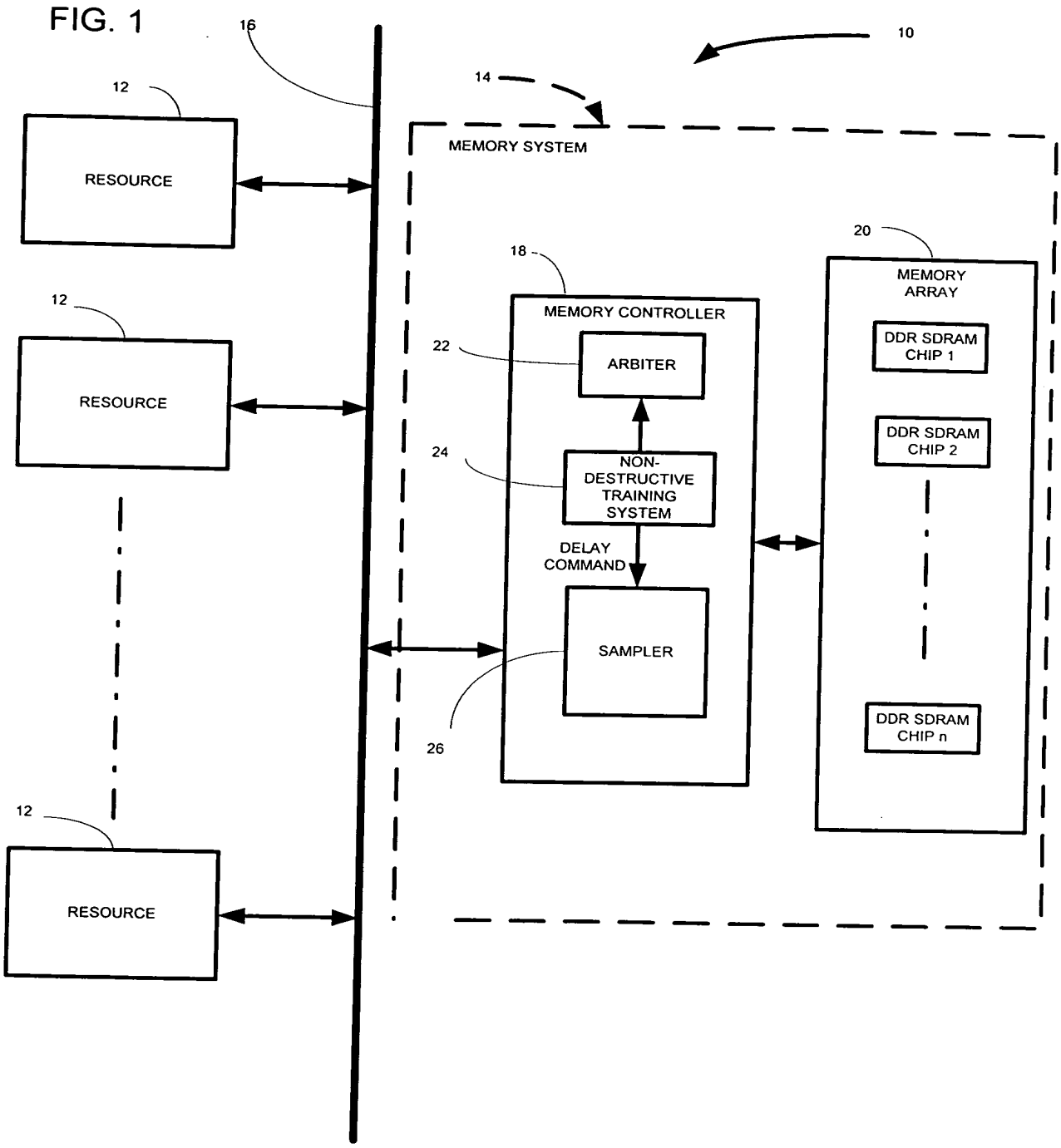
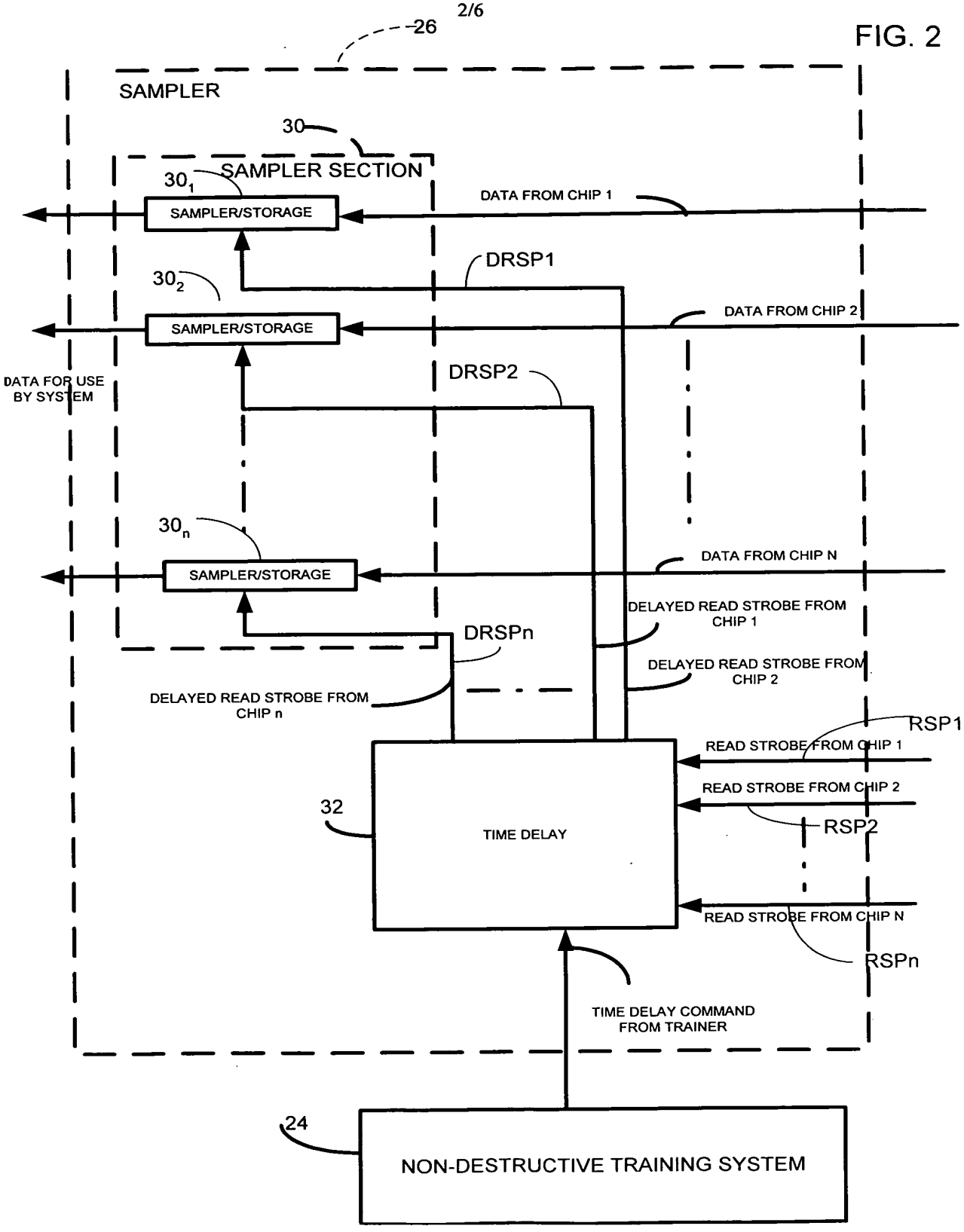

16
10
14
12
RESOURCE
MEMORY SYSTEM
18
20
MEMORY CONTROLLER
MEMORY ARRAY
22
ARBITER
DDR SDRAM CHIP 1
DDR SDRAM CHIP 2
24
NON-DESTRUCTIVE TRAINING SYSTEM
DELAY COMMAND
SAMPLER
26
DDR SDRAM CHIP n

FIG. 2


26
SAMPLER
30
SAMPLER SECTION
30_1
SAMPLER/STORAGE
DATA FROM CHIP 1
DRSP1
30_2
SAMPLER/STORAGE
DATA FROM CHIP 2
DRSP2
DATA FOR USE BY SYSTEM
30_n
SAMPLER/STORAGE
DATA FROM CHIP N
DELAYED READ STROBE FROM CHIP 1
DRSPn
DELAYED READ STROBE FROM CHIP 2
DELAYED READ STROBE FROM CHIP n
RSP1
READ STROBE FROM CHIP 1
READ STROBE FROM CHIP 2
32
TIME DELAY
RSP2
READ STROBE FROM CHIP N
RSPn
TIME DELAY COMMAND FROM TRAINER
24
NON-DESTRUCTIVE TRAINING SYSTEM

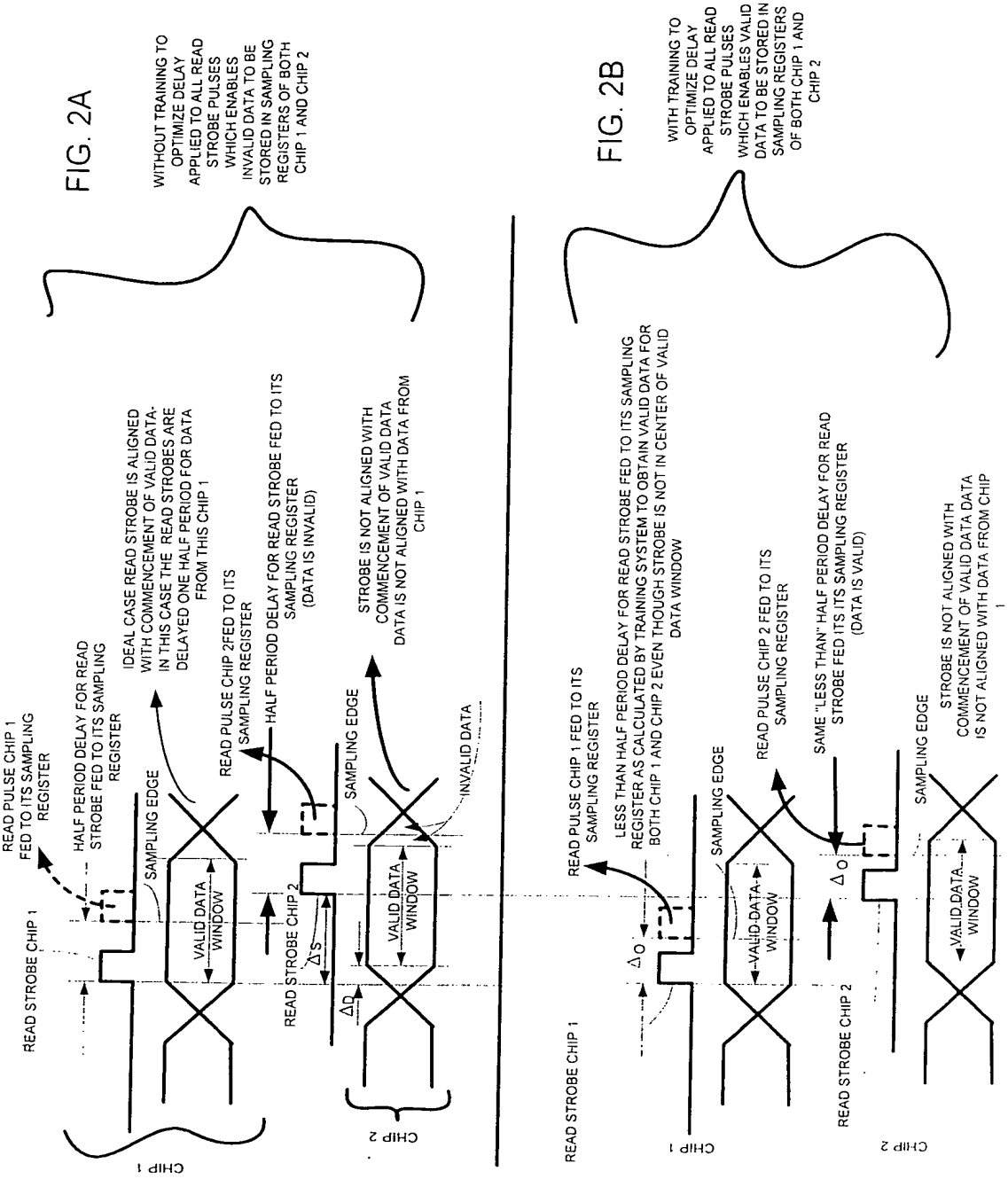


FIG. 2A
WITHOUT TRAINING TO OPTIMIZE DELAY APPLIED TO ALL READ STROBE PULSES WHICH ENABLES INVALID DATA TO BE STORED IN SAMPLING REGISTERS OF BOTH CHIP 1 AND CHIP 2
READ PULSE CHIP 1 FED TO ITS SAMPLING REGISTER
HALF PERIOD DELAY FOR READ STROBE FED TO ITS SAMPLING REGISTER
IDEAL CASE READ STROBE IS ALIGNED WITH COMMENCEMENT OF VALID DATA- IN THIS CASE THE READ STROBES ARE DELAYED ONE HALF PERIOD FOR DATA FROM THIS CHIP 1
READ PULSE CHIP 2FED TO ITS SAMPLING REGISTER
HALF PERIOD DELAY FOR READ STROBE FED TO ITS SAMPLING REGISTER (DATA IS INVALID)
STROBE IS NOT ALIGNED WITH COMMENCEMENT OF VALID DATA DATA IS NOT ALIGNED WITH DATA FROM CHIP 1
SAMPLING EDGE
SAMPLING EDGE
INVALID DATA
VALID DATA WINDOW
VALID DATA WINDOW
READ STROBE CHIP 1
READ STROBE CHIP 2
ΔS
ΔD
CHIP 1
CHIP 2
FIG. 2B
WITH TRAINING TO OPTIMIZE DELAY APPLIED TO ALL READ STROBE PULSES WHICH ENABLES VALID DATA TO BE STORED IN SAMPLING REGISTERS OF BOTH CHIP 1 AND CHIP 2
READ PULSE CHIP 1 FED TO ITS SAMPLING REGISTER
LESS THAN HALF PERIOD DELAY FOR READ STROBE FED TO ITS SAMPLING REGISTER AS CALCULATED BY TRAINING SYSTEM TO OBTAIN VALID DATA FOR BOTH CHIP 1 AND CHIP 2 EVEN THOUGH STROBE IS NOT IN CENTER OF VALID DATA WINDOW
READ PULSE CHIP 2 FED TO ITS SAMPLING REGISTER
SAME "LESS THAN" HALF PERIOD DELAY FOR READ STROBE FED ITS ITS SAMPLING REGISTER (DATA IS VALID)
STROBE IS NOT ALIGNED WITH COMMENCEMENT OF VALID DATA DATA IS NOT ALIGNED WITH DATA FROM CHIP 1
SAMPLING EDGE
SAMPLING EDGE
VALID DATA WINDOW
VALID DATA WINDOW
READ STROBE CHIP 1
READ STROBE CHIP 2
ΔO
ΔO
CHIP 1
CHIP 2

FIG. 3

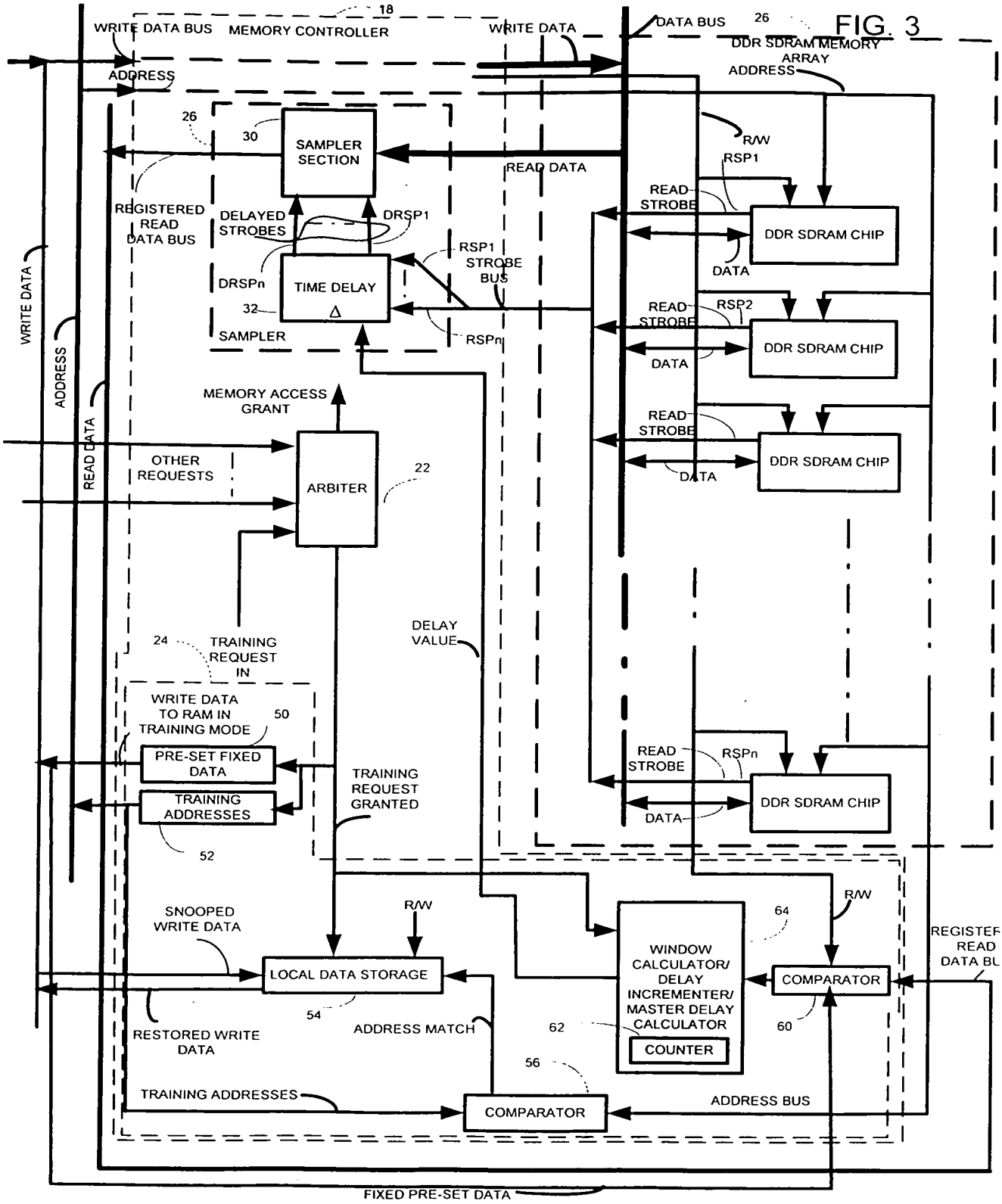

18
WRITE DATA BUS
MEMORY CONTROLLER
WRITE DATA
DATA BUS
26
DDR SDRAM MEMORY ARRAY
ADDRESS
ADDRESS
26
30
SAMPLER SECTION
R/W
RSP1
READ DATA
READ STROBE
REGISTERED READ DATA BUS
DELAYED STROBES
DRSP1
DDR SDRAM CHIP
DATA
RSP1 STROBE BUS
DRSPn
TIME DELAY
Δ
32
SAMPLER
RSPn
READ STROBE
RSP2
DDR SDRAM CHIP
DATA
WRITE DATA
ADDRESS
READ DATA
MEMORY ACCESS GRANT
READ STROBE
OTHER REQUESTS
ARBITER
22
DDR SDRAM CHIP
DATA
DELAY VALUE
24
TRAINING REQUEST IN
WRITE DATA TO RAM IN TRAINING MODE
50
PRE-SET FIXED DATA
TRAINING ADDRESSES
52
TRAINING REQUEST GRANTED
READ STROBE
RSPn
DDR SDRAM CHIP
DATA
R/W
64
R/W
SNOOPED WRITE DATA
LOCAL DATA STORAGE
54
WINDOW CALCULATOR/ DELAY INCREMENTER/ MASTER DELAY CALCULATOR
COUNTER
62
COMPARATOR
60
REGISTER READ DATA BU
RESTORED WRITE DATA
ADDRESS MATCH
56
TRAINING ADDRESSES
COMPARATOR
ADDRESS BUS
FIXED PRE-SET DATA

FIG. 4

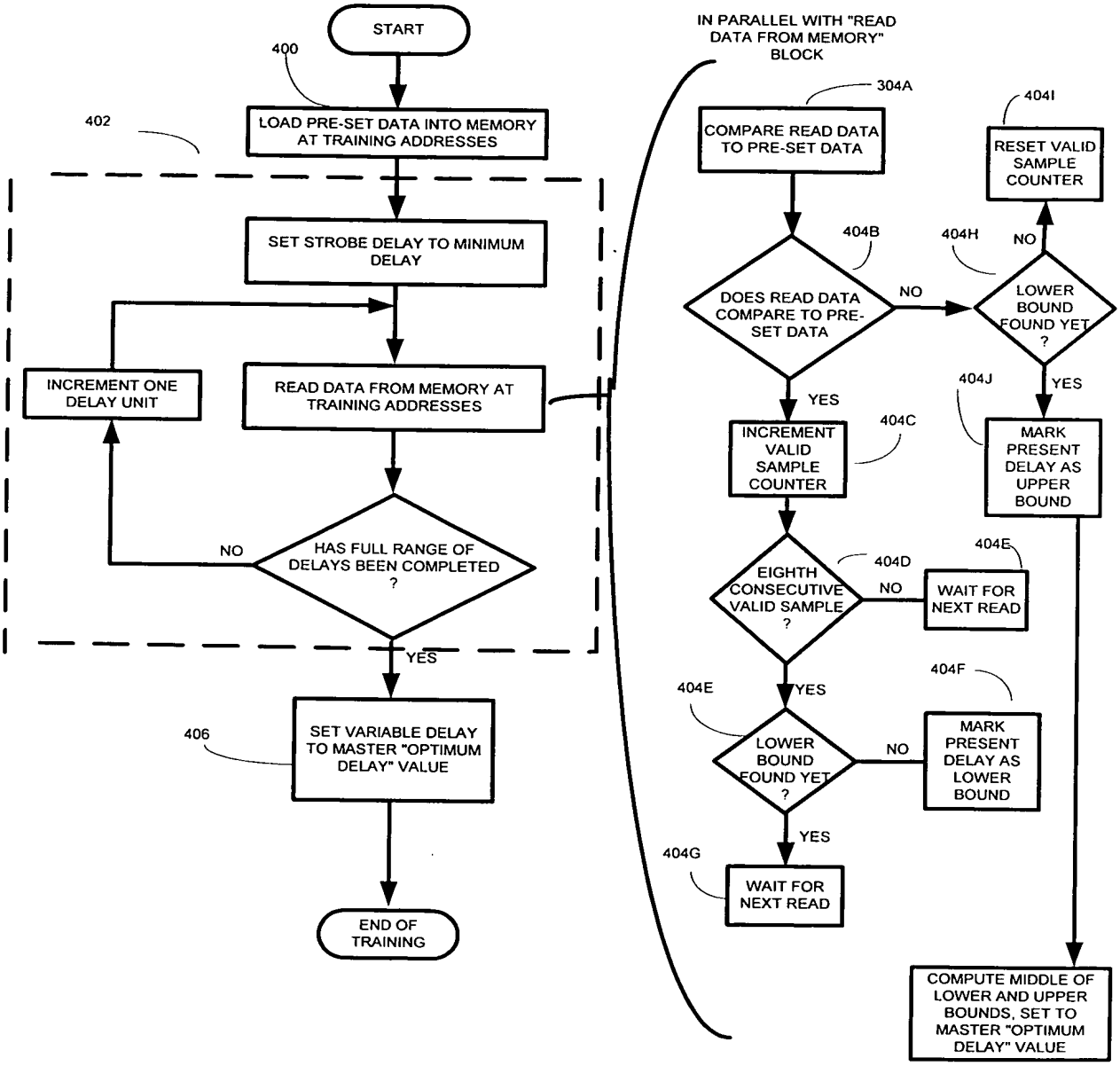
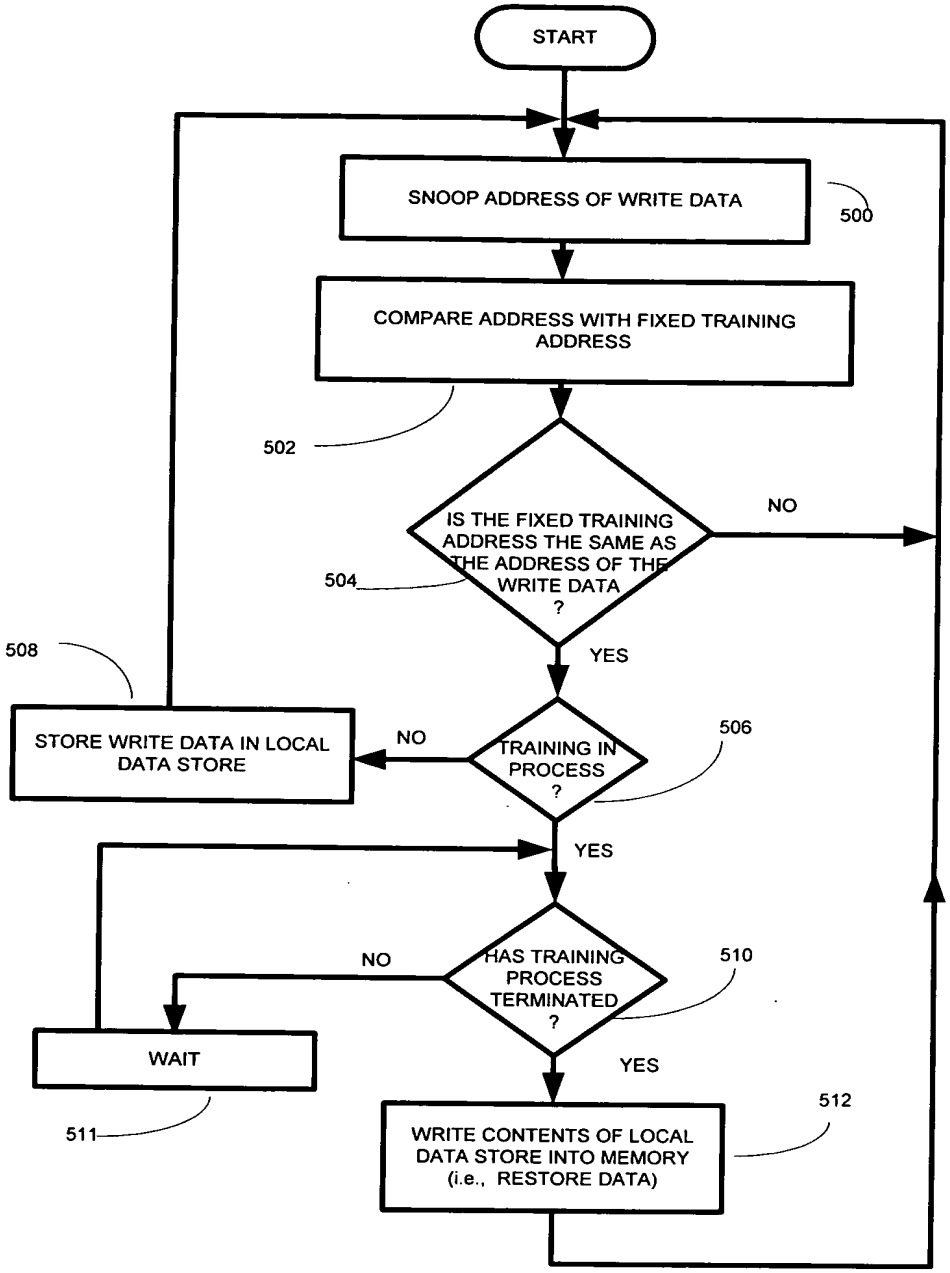

START
400
LOAD PRE-SET DATA INTO MEMORY AT TRAINING ADDRESSES
402
SET STROBE DELAY TO MINIMUM DELAY
INCREMENT ONE DELAY UNIT
READ DATA FROM MEMORY AT TRAINING ADDRESSES
NO
HAS FULL RANGE OF DELAYS BEEN COMPLETED ?
YES
406
SET VARIABLE DELAY TO MASTER "OPTIMUM DELAY" VALUE
END OF TRAINING
IN PARALLEL WITH "READ DATA FROM MEMORY" BLOCK
304A
COMPARE READ DATA TO PRE-SET DATA
404B
DOES READ DATA COMPARE TO PRE-SET DATA
NO
404H
LOWER BOUND FOUND YET ?
NO
404I
RESET VALID SAMPLE COUNTER
YES
404J
MARK PRESENT DELAY AS UPPER BOUND
YES
404C
INCREMENT VALID SAMPLE COUNTER
404D
EIGHTH CONSECUTIVE VALID SAMPLE ?
NO
404E
WAIT FOR NEXT READ
YES
404E
LOWER BOUND FOUND YET ?
NO
404F
MARK PRESENT DELAY AS LOWER BOUND
YES
404G
WAIT FOR NEXT READ
COMPUTE MIDDLE OF LOWER AND UPPER BOUNDS, SET TO MASTER "OPTIMUM DELAY" VALUE

FIG. 5


START
SNOOP ADDRESS OF WRITE DATA
500
COMPARE ADDRESS WITH FIXED TRAINING ADDRESS
502
IS THE FIXED TRAINING ADDRESS THE SAME AS THE ADDRESS OF THE WRITE DATA ?
504
NO
YES
508
STORE WRITE DATA IN LOCAL DATA STORE
NO
TRAINING IN PROCESS ?
506
YES
NO
HAS TRAINING PROCESS TERMINATED ?
510
WAIT
511
YES
512
WRITE CONTENTS OF LOCAL DATA STORE INTO MEMORY (i.e., RESTORE DATA)